REMARKS

Status of Claims

The Applicant has received and reviewed the non-final Office Action mailed June 27, 2007. The Applicant originally submitted claims 1-12 in this application. By the present Response and Amendment, the Applicant has amended claims 1, 5 and 8, but has not canceled any claims. Thus, claims 1-12 remain pending in this application.

Specification

The Examiner reminded the Applicant of the proper language and format for the Abstract of the Disclosure. In response, the Applicant has amended the Abstract to be within the range of 50 to 150 words and to be clear and concise and not include phrases that can be implied. In view of the amendments to the Abstract, the Applicant respectfully submits that the Abstract now includes proper language and is in proper format.

Objection of Drawings

The drawings are objected to because of their failure to include reference signs 73 and 75 mentioned in paragraphs [0023] and [0024] of the Applicant's description. In response to the objection, the Applicant has submitted herewith a corrected FIG. 2, in which the second high to low transition 73, which had been improperly labeled originally, has been corrected by changing the improper reference sign "72" to the proper reference sign "73". With respect to the reference sign 75, the Applicant respectfully notes that the connection 75 is properly shown and labeled in FIG. 1. In view of the corrected drawings submitted herewith and the Applicant's remarks, the Applicant respectfully submits that the drawings no longer are objectionable. Accordingly, the Applicant respectfully requests that the drawing objection be withdrawn.

Rejection of Claim 5 under 35 U.S.C. §112, first paragraph

The Examiner rejected claim 5 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. More specifically, the Examiner indicated that the Applicant's specification describes the invalid data as having a duration less than the clock cycle setting, but claim 5 recites the invalid data as having a duration greater than the clock cycle setting. In response to the rejection, the Applicant has amended claim 5 to recite that the invalid data comprises data that has changed logical state for a duration less than the clock cycle setting. Support for the claim amendment can be found in the Applicant's specification, e.g., in paragraph [0016]. In view of the claim amendment, the Applicant respectfully submits that the claim is consistent with the description, and therefore the claim no longer fails to meet the enablement requirement. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejection.

Rejection of Claims 1, 4, 8 and 9 under 35 U.S.C. §102(b)

The Examiner rejected claims 1, 4, 8 and 9 under 35 U.S.C. §102(b) as being anticipated by Anderson et al. (U.S. Patent No. 5,457,718). The Applicant respectfully traverses this rejection in view of the claim amendments above and the remarks set forth below.

The Anderson et al. reference discloses a digital filter for use in a phase lock loop (PLL) to synchronize various clock signals, e.g., an input data signal, with a local clock signal. The cited portion of Anderson et al. (FIG. 1) discloses a retiming circuit for retiming a data input signal with respect to a local clock signal. In FIG. 1, a digital filter (40) interacts with a phase comparator (30) to provide a phase lock loop for retiming the input data signal, i.e., for retiming the phase of the input data signal with the phase of the local clock signal. More specifically, the phase comparator (30) compares the phase of the input data signal with the phase of the local clock signal. The difference in phase is output by the phase comparator (30) to the digital filter (40), which provides a feedback signal that controls the delay of the variable delay circuit (20). Based on the phase difference between the input data signal and the local clock signal, as determined

by the phase comparator (30) and its corresponding output signal to the digital filter (40), the feedback signal from the digital filter (40) to the variable delay circuit (20) controls the amount by which the variable delay circuit (20) delays the phase of the input data signal. This feedback loop between the variable delay circuit (20), the phase comparator (30) and the digital filter (40) adjusts the phase of the input data signal until the input data signal is in phase with the local clock signal.

The Examiner cites the variable delay element (20) in Anderson et al. as disclosing the Applicant's digital delay element (12), the phase comparator (30) in Anderson et al. as disclosing the Applicant's comparator (14), and the digital filter (40) and col. 3, lines 59-67 as disclosing the Applicant's final stage (16). Initially, the Applicant notes that the Anderson et al. reference uses a retiming circuit comprising a variable delay element (20), a phase comparator (30) and a digital filter (40) to retime the phase of an input data signal with the phase of a local clock signal. The Applicant's invention, as recited in independent claims 1 and 8, uses a digital filtering apparatus (10) comprising a digital delay element (12), a comparator (14) and a final stage (16) to filter out invalid data, which is data that does not maintain the same logical state for a duration greater than the clock cycle setting of the digital filtering apparatus. Therefore, even at this relatively basic level of comparison, it is clear that the FIG. 1 retiming circuit of Anderson et al. is an entirely different apparatus from the Applicant's digital filtering apparatus, and the FIG. 1 retiming circuit of Anderson et al. performs an entirely different function than the Applicant's digital filtering apparatus.

Moreover, the content and organization of the cited elements in Anderson et al. clearly do not coincide with those of the Applicant's invention, and therefore can not possibly disclose or suggest the Applicant's invention. For example, in Anderson et al., the retiming circuit includes both a phase comparator and a digital filter, among other components. In the Applicant's claimed invention, a comparator is part of the digital filtering apparatus, not a separate component from the digital filtering apparatus. More specifically, the phase comparator (30) in Anderson et al. compares the phase of an input data signal to the phase of a local clock signal. The Applicant's comparator (14) compares the outputs of each of the delay components within the digital delay element (12) to determine whether all of the delay component outputs have the same logical

state, which the comparator determines as being indicative of valid data clocking through the digital delay element. The phase comparator (30) in Anderson et al. is not comparing the outputs of components within the delay element, nor is there any suggestion to do such comparison.

Also, the digital filter (40) in Anderson et al. uses the output of the phase comparator (30) to provide a feedback control signal to the variable delay element (20) to delay the input data signal by an appropriate amount. Delaying the input data signal is used to synchronize the phase of the input data signal with the phase of the local clock signal. The Applicant's digital filtering apparatus (10) is not a component within the overall apparatus. Rather, the Applicant's digital filtering apparatus (10) is the overall apparatus, which filters out spurious or invalid data, i.e., data that does not maintain its logical state for a duration greater than the clock cycle setting. Nothing in Anderson et al. discloses or suggests the digital filter (40) or any other component in the retiming circuit of Anderson et al. filtering out spurious or invalid data, especially in the manner of the Applicant's digital filtering apparatus (10). As discussed hereinabove, the retiming circuit in Anderson et al. is used to synchronize the phase of an input data signal with the phase of a local clock signal.

The Applicant has amended independent claims 1 and 8 to clarify existing distinctions between the Applicant's invention and Anderson et al. More specifically, the Applicant has amended independent claims 1 and 8 to recite that the comparator compares the output of each of the plurality of delay components within the digital delay element. Also, the Applicant has amended independent claims 1 and 8 to recite that the comparator recognizes data clocking through the delay element as invalid data if the outputs of each of the plurality of delay components within the digital delay element are not the same logical state, and as valid data if the outputs of each of the plurality of delay components within the digital delay element are the same logical state. Support for the claim amendments is found in the Applicant's specification, e.g., in paragraph [0021].

In view of the claim amendments, and for at least the reasons discussed hereinabove, the Applicant respectfully submits that the Anderson et al. reference does not disclose or suggest the Applicant's invention, as recited in independent claims 1 and

8, as amended. Claim 4, which depends from claim 1, and claim 9, which depends from claim 8, likewise are not disclosed or suggested by Anderson et al. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 4, 8 and 9 under 35 U.S.C. §102(b) as being anticipated by Anderson et al.

Rejection of Claims 2, 3, 6, 7, 10 and 12 under 35 U.S.C. §103(a)

The Examiner rejected claims 2, 3, 6, 7, 10 and 12 under 35 U.S.C. §103(a) as being unpatentable over Anderson et al. in view of Clements et al. (U.S. Patent Pub. No. 2005/0105507). The Applicant respectfully traverses this rejection in view of the remarks set forth below.

The rejected claims 2, 3, 6 and 7 depend directly from independent claim 1, and incorporate all of the features of claim 1. The rejected claims 10 and 12 depend directly from independent claim 8, and incorporate all of the features of claim 8.

As discussed above with respect to claims 1 and 8, as amended, the Applicant's claimed invention is neither disclosed in nor suggested by Anderson et al. The Clements et al. reference, which is cited for its disclosure of the use of a plurality of flip-flops within a digital delay element, does not cure the deficiencies of Anderson et al. with respect to disclosing or suggesting the Applicant's claimed invention. Accordingly, the Applicant respectfully submits that the Clements et al. reference, taken either alone or in combination with Anderson et al., does not disclose or suggest the Applicant's invention, as recited in independent claims 1 and 8.

Since the rejected claims 2, 3, 6 and 7 depend directly from independent claim 1, and incorporate all of the features of claim 1, and since the rejected claims 10 and 12 depend directly from independent claim 8, and incorporate all of the features of claim 8, the Applicant respectfully submits that the Clements et al. reference, taken either alone or in combination with Anderson et al., does not disclose or suggest the Applicant's invention, as recited in dependent claims 2, 3, 6, 7, 10 and 12. Furthermore, claims 2, 3, 6, 7, 10 and 12 include other features that, when combined with the subject matter of their respective independent claim, are neither shown in nor suggested by the art of record. Therefore, the Applicant respectfully requests that the Examiner withdraw the

rejection of claims 2, 3, 6, 7, 10 and 12 under 35 U.S.C. §103(a) as being unpatentable over Anderson et al. in view of Clements et al.

Rejection of Claims 6 and 11 under 35 U.S.C. §103(a)

The Examiner rejected claims 6 and 11 under 35 U.S.C. §103(a) as being unpatentable over Anderson et al. in view of Clements et al. and Byram et al. (U.S. Patent No. 3,829,798). The Applicant respectfully traverses this rejection in view of the remarks set forth below.

As discussed previously herein, the Applicant's claimed invention recited in independent claims 1 and 8, as amended, is neither disclosed in nor suggested by Anderson et al. The Byram et al. reference, which is cited for its disclosure of using delay elements to adjust the bandwidth of a filter, does not cure the deficiencies of Anderson et al. and Clements et al. with respect to disclosing or suggesting the Applicant's claimed invention. Accordingly, the Applicant respectfully submits that the Byram et al. reference, taken either alone or in combination with Anderson et al. and Clements et al., does not disclose or suggest the Applicant's invention, as recited in independent claims 1 and 8.

The rejected claims 6 and 11 depend directly from independent claims 1 and 8, respectively, and incorporate all of the features of their respective independent claim. Furthermore, claims 6 and 11 include other features that, when combined with the subject matter of their respective independent claim, are neither shown in nor suggested by the art of record. Therefore, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 6 and 11 under 35 U.S.C. §103(a) as being unpatentable over Anderson et al. in view of Clements et al. and Byram et al.

CONCLUSION

For at least the reasons set forth above, the Applicant respectfully submits that all pending claims are in condition for allowance. The Applicant respectfully requests reconsideration of the rejections and allowance of the application. Should there be any further questions or concerns, the Examiner is urged to telephone the undersigned to expedite prosecution.

Respectfully submitted,
SMITH FROHWEIN TEMPEL
GREENLEE BLAHA LLC

By: /John M. Harman/
John M. Harman, Reg. No. 38,173

SMITH FROHWEIN TEMPEL GREENLEE BLAHA LLC
Two Ravinia Drive, Suite 700
Atlanta, Georgia 30346
Phone: 404.815.9300
Fax: 770.804.0900